Synchronization of single-channel stepper motor drivers reduces noise and interference

In most applications, a non-synchronized operation causes no problems.

However, in some cases the switching of the two channels interfere, causing audible noise and vibrations from the motor. By synchronizing the switching in the two channels, interference and noise will be cancelled.

Synchronization of New JRC´s stepper motor drivers

The single channel stepper motor drivers NJM3717 and NJM3770A are not synchronized in the typical application of fig. 1, i.e. the PWM switching of one channel is totally independent of the other cannel. Note that the Dual channel drivers (NJM3771/ 3772/ 3773/3774 and 3775) all are synchronized by design. The basic operation of the PWM switching is described in the data sheet of each circuit.

Improvements by synchronization

From the electrical point of view, synchronization 180° out of phase gives some major improvements. With two channels free-running, the peak supply current will be the sum of the current in the two channels, as shown in figure 2. When synchronized 180° out of phase, the two channels will never be on at the same time. Peak supply current is then equal to the peak value of one channel. Higher-order harmonics will also be significantly reduced in amplitude. This means a reduced need for power supply filtering, or better filtering from the same filtering components. Magnetically coupled noise to nearby circuitry will also be reduced as the peak current and higher order harmonics are reduced.

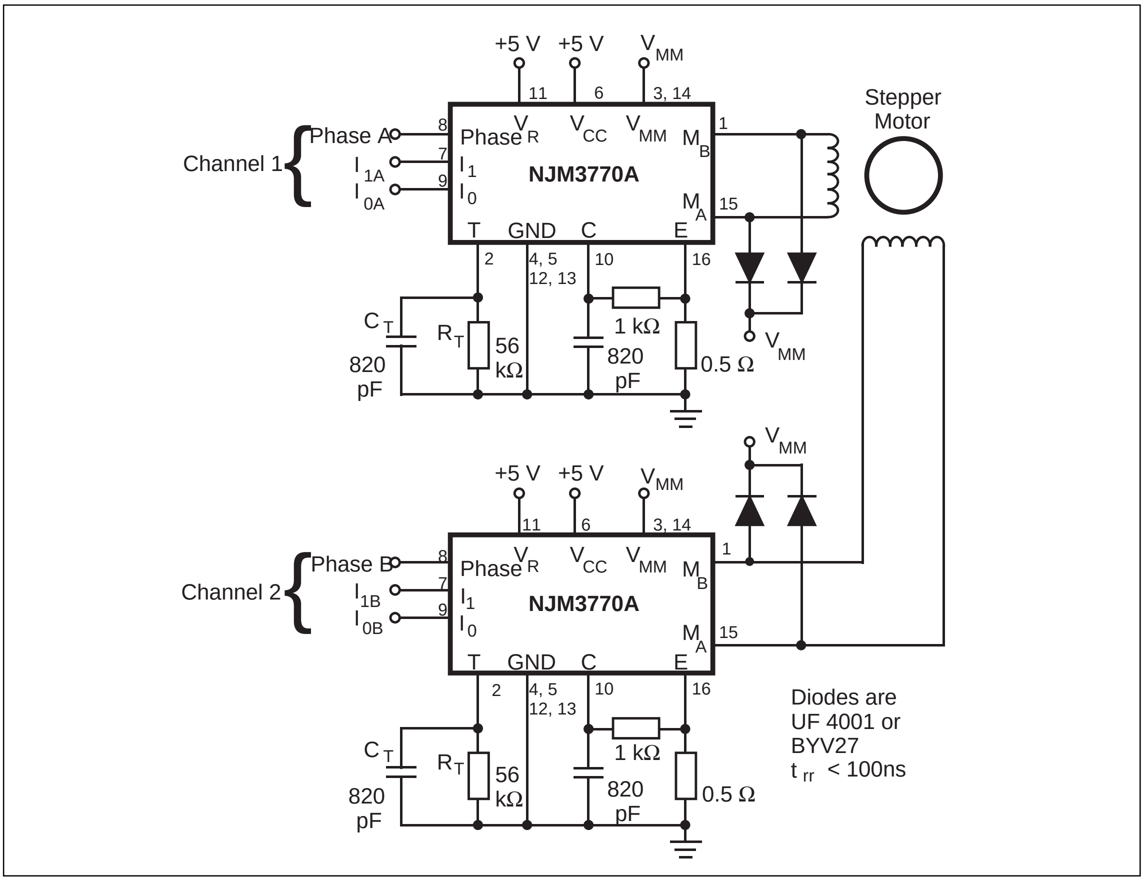

Figure 1. Typical stepper motor driver application with NJM3770A.

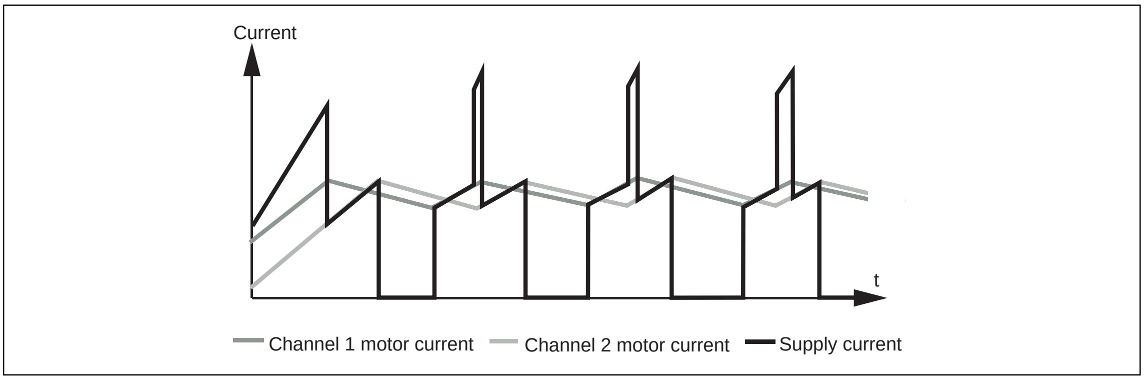

Figure 2. Typical supply current with two channels free-running.

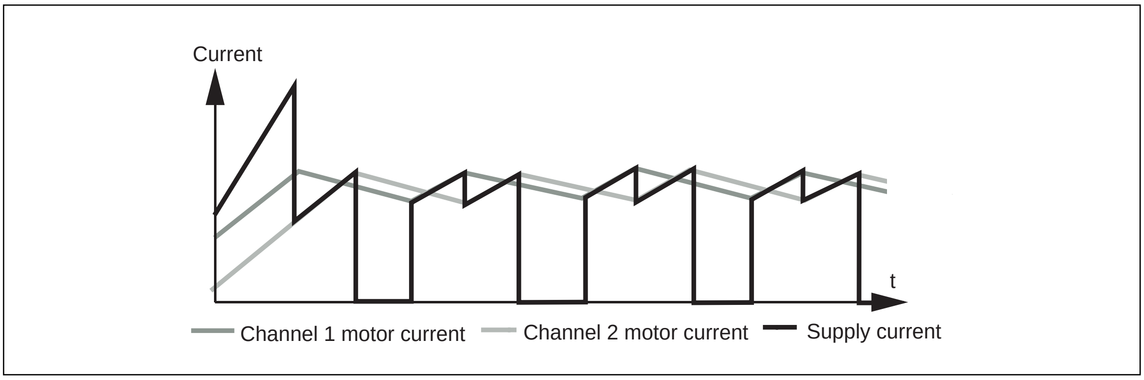

Figure 3. Timing diagram with two channels during synchronized operation.

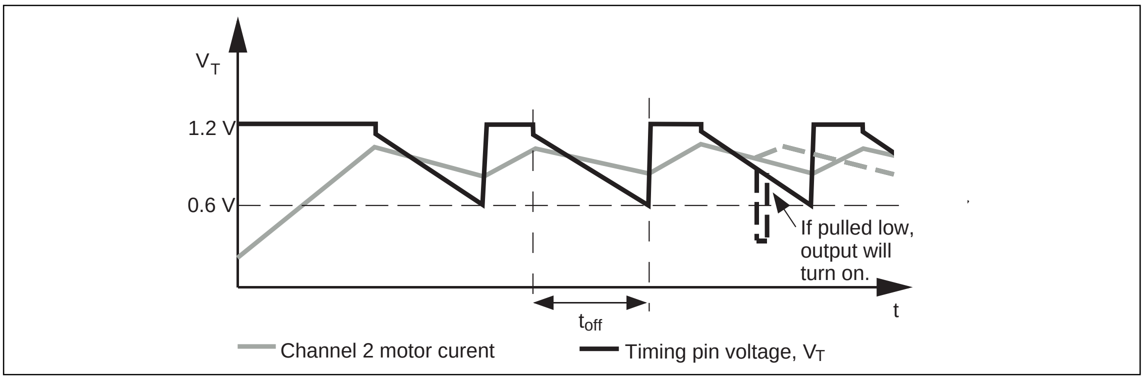

Figure 4. Motor current and V_T voltage vs.time.

The design

Fig. 3 shows the timing diagram during synchronized operation. Channel 1 is designated the master, and channel 2 the slave. When synchronized, the off-time of the slave will not be controlled by the internal monostable flip-flop, but by the turn-off of the master. By increasing the timing capacitor value C_T (and thereby increasing the off-timeof the slave), the master will always give the turn-on trigger pulse before the monostable. As long as the total duty cycle (the sum of channel 1 & 2 duty cycles), are less than 100%, the two channel will never be turned on simultaneously.

The operation of the monostable flip-flop is shown in fig 4. In the motor current output-on state, the V_T voltage is constantly kept at about 1.2 V at the T (Timing) pin. When the motor peak current is reached, the monostable flip-flop is triggered, and V_T decreases as C_T discharges through R_T. At V_T=0.6 V a comparator resets the monostable flip-flop, and turns the output on again. An external sinking output connected to the T-pin could discharge C_T in a very short time, and induce an immediate turn-on.

The circuit diagram is shown in figure 5. A 4093 CMOS Schmitt trigger NAND-gate and some external components form an edge detector to generate the sync pulses.

Gate #1 detects the off-state of channel 1. The voltage divider resistor network including R1 and R2 reduces the input voltage swing to equal the 4093 supply voltage. If V_{MM} is below 15 V, 4093 can be fed by V_{MM}, and the voltage divider network could be omitted.

In the off-state both M_{A1} and M_{A2} are high (=V_{MM}) giving a low output of gate #1. Gate #2 inverts the signal, and sends it through a high pass filter, acting as a positive edge detector. For each positive transition of gate #2 (occurring when channel 1 is turned off), a short negative pulse is generated at the output of gate #3. The other input of gate #3 (Sync) may be used as a disable input. The diode at the output of gate #3 makes it a sinking output. At each negative pulse at gate #3 output, the C_T capacitor of 1.5 nF is discharged, and the output of the driver accordingly turned on.

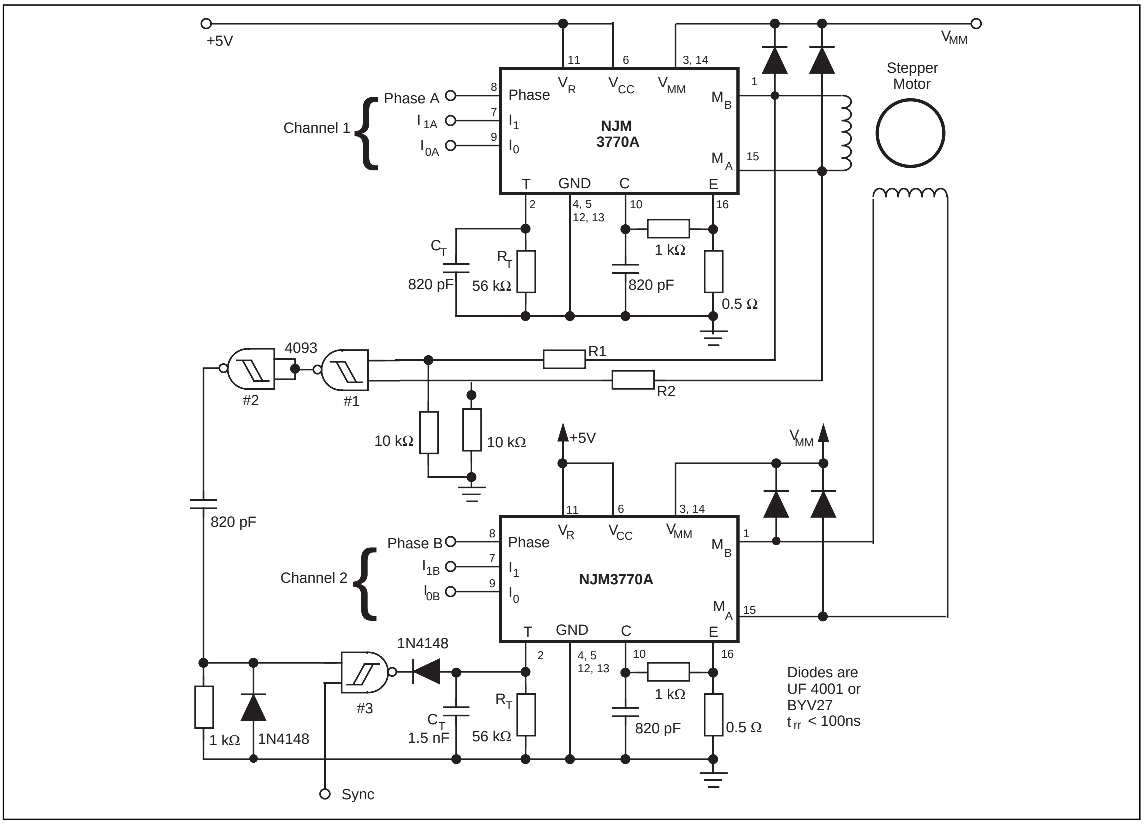

Figure 5. Two NJM3770A in synchronized operation using a master/slave configuration.

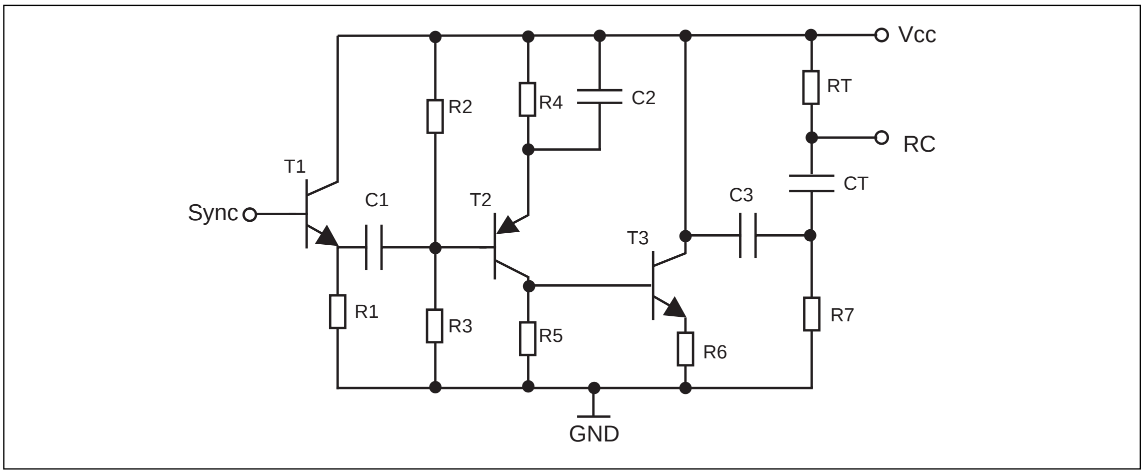

Figure 6. Synchronising circuit Schematics.

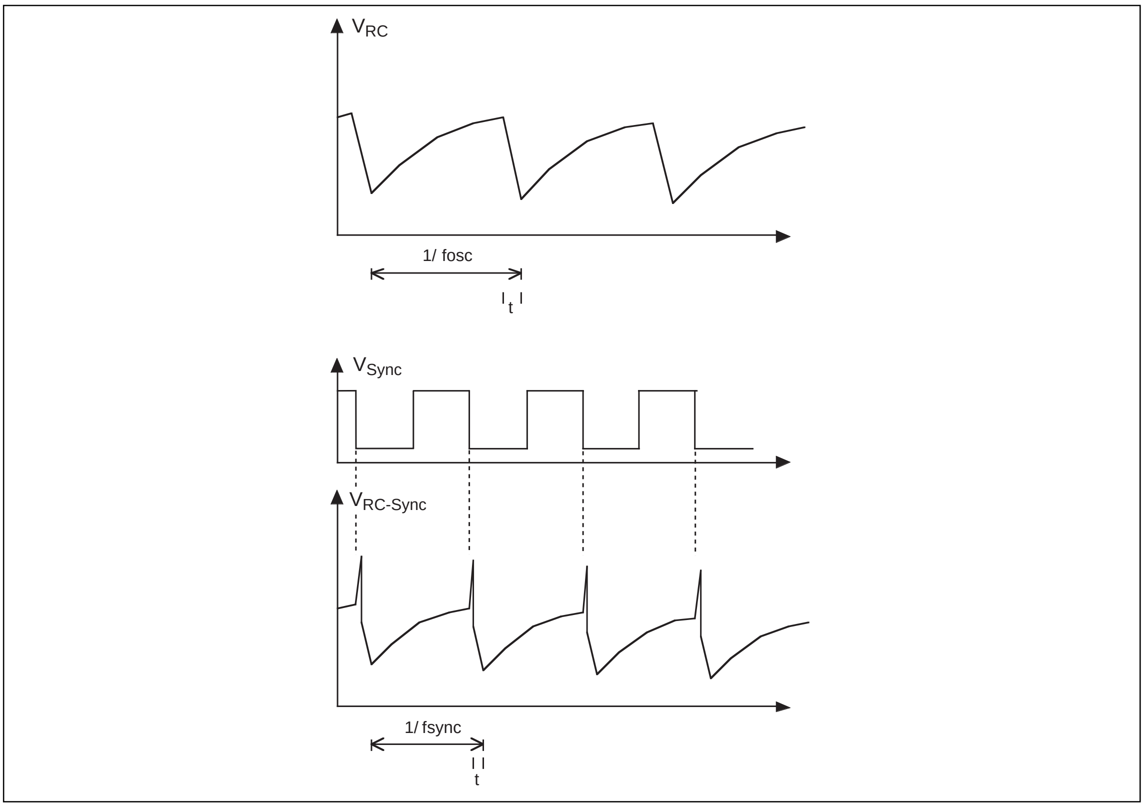

Figure 7. Signal at the RC input and sync pulse, without sync pulse, sync pulse and with syncpulse.

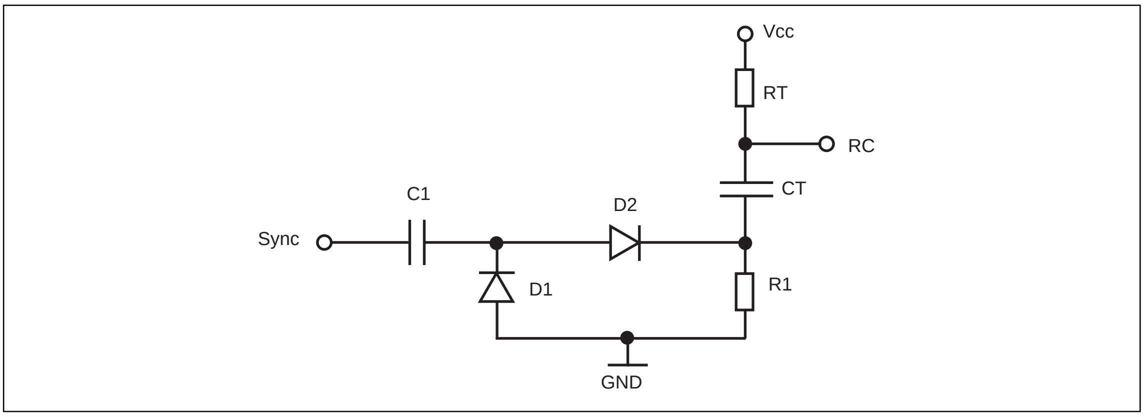

Figure 8. Synchronise circuit for an square wave sync signal.

Synchronising the RC Oscillator On NJM3771 to NJM3777

Method 1

To synchronise the RC oscillator with an external signal You will need some extra transistors, resistors and capacitors. The synchronising circuit in figure 6 works to synchronise two RC oscillators or to synchronise the RC oscillator with an external sync pulse.

The free RC oscillator frequency must be lower than the sync frequency. For component value se table below.

T1, T3	BC548B
T2	BC558B
R1,R5	1k resistor
R2,R3,R4	10k resistor
R6	470k resistor
R7	24 resistor
RT,CT	Should be chosen after the sync. frequency.

In order to get the sync circuit to work properly the free oscillator frequency should be as close as possible to the sync frequency. It is also important that the negative slope of the RC signal (see figure 7) is minimum 1 µs in order to have the RS flip flop in the stepper motor driver circuit set.

To calculate your free oscillator frequency f_{osc} you can use the approximation formula below:

$f_{osc} = 1 / (0.77 \cdot R_T \cdot C_T)$

If your time t (see figure 7) is to short, less than 1 µs, then you can enlarge it by increasing the value of C_T and at the same time decrease the value of R_T to keep the same frequency f_{osc}.

This method is also useful if you want to synchronise two RC oscillators. You must chose one to be the master and the other to be slave. The master oscillator must have a higher frequency than the slave oscillators. The same synchronise circuit as in figure 6 can be used.

Method 2

With one capacitor and two diodes you can synchronise the RC oscillator with an external square wave.

C1	=	10 nF
D1,D2	=	1N4148
R1	=	24 Ω.